

# Chinese Microwave Synthesiser PCBs Using ADF4351 and the ADF5355

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# Overview of Talk

- Brief review of PLL chips with integrated VCOs.
- Look at what is readily available.
- Background on Int and Frac-N PLLs.
- How to use these chips.
- Overcoming some of the weaknesses of the Chinese PCBs.

# Synthesiser Chips with on-chip VCOs

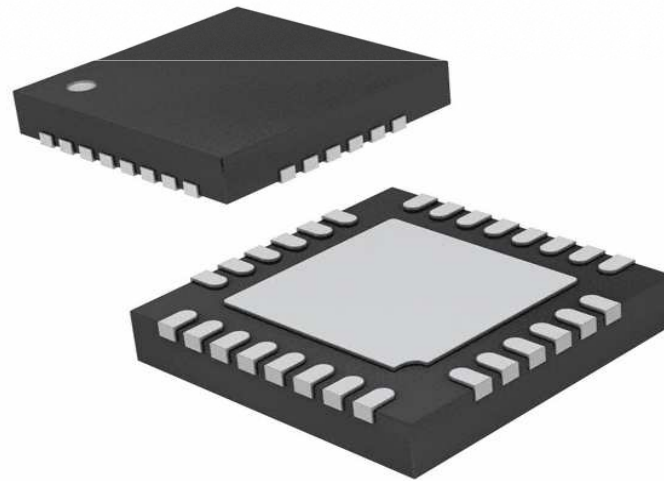
- Over past six years a number of frequency synthesisers have become available with on-chip VCOs operating in the microwave region of the spectrum
- These make the implementation of microwave signal sources relatively straight forward
- There are some drawbacks (of course!)
- This talk will look at these and discuss ways round them.

# Synthesiser Chips with on-chip VCOs

- Analog Devices ADF4350, ADF4351
  - 35 MHz to 4.3 GHz and 54 MHz to 13.6 GHz.
- Analog Devices ADF5355 and ADF5356
  - 54 MHz to 13.6 GHz.
- TI LMX 2541 (Ex Nat Semi)
  - 31.6 MHz to 4.0 GHz
- Linear Technology LT6948 (Now AD)
  - 37 MHz to 6.39 GHz

# Chip packages

- Typically these chips are packaged in 32-pin Lead Frame Chip Scale Package [LFCSP] package and are difficult to solder.



# Fortunately they are available from China on Ebay


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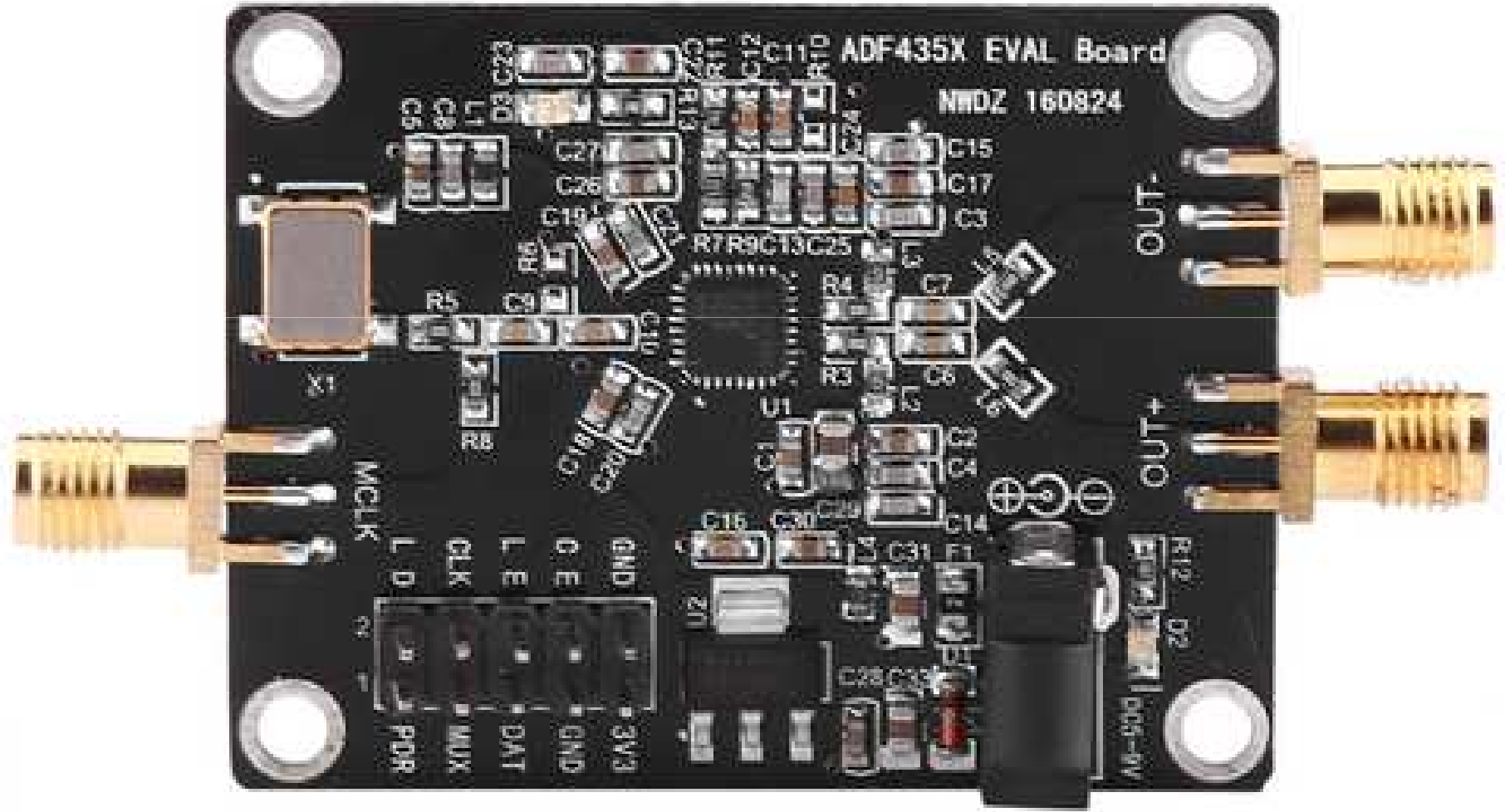
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# Chinese ADF4351 PCB

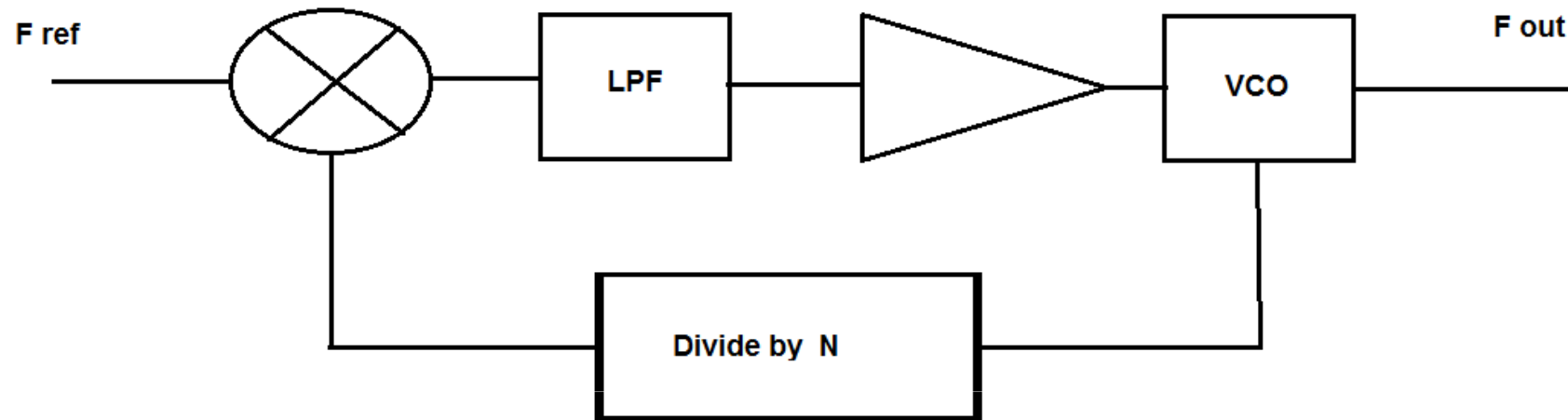




# Int-N and Frac-N PLLs

- These chips use Fractional-N PLLs
- Allows very small tuning steps
- Allows the use of much higher phase detector frequencies.
- Can give better phase noise (PN) performance.
- What is the difference between Frac-N and Int-N ???

# Basic Int-N PLL

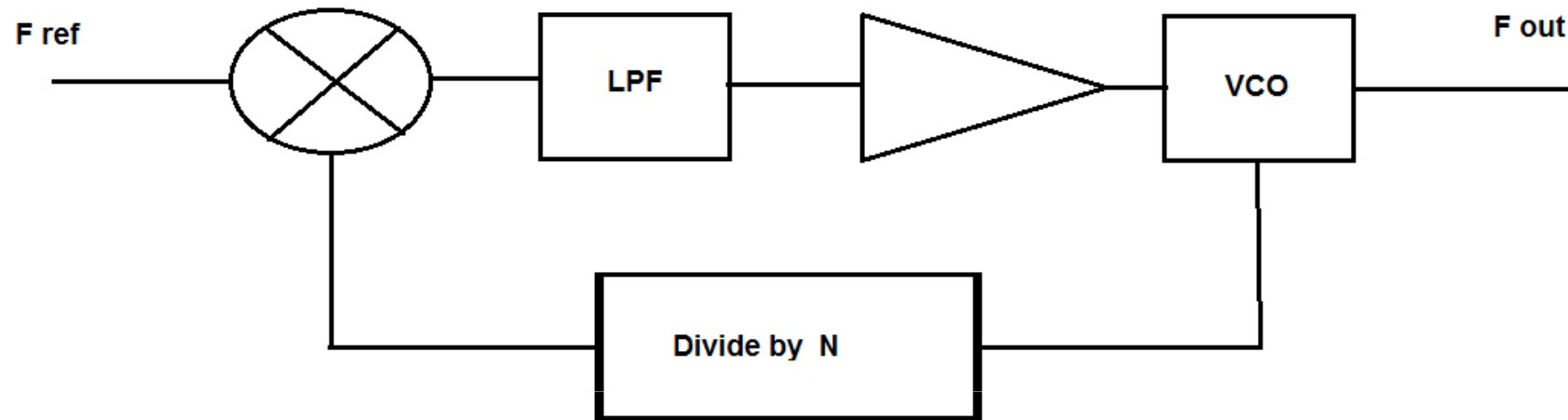


$$F_{out} = N \cdot F_{ref}$$

$$F_{out} = 1, 2, 3, \dots, n \cdot F_{ref}$$

If  $N$  is an integer minimum step size of  $F_{out}$  is  $F_{ref}$

# Frac-N PLL



$$F_{out} = N \cdot F_{ref}$$

$N$  need not be an integer and can be a fractional number. This opens up useful possibilities for the design of the PLL.

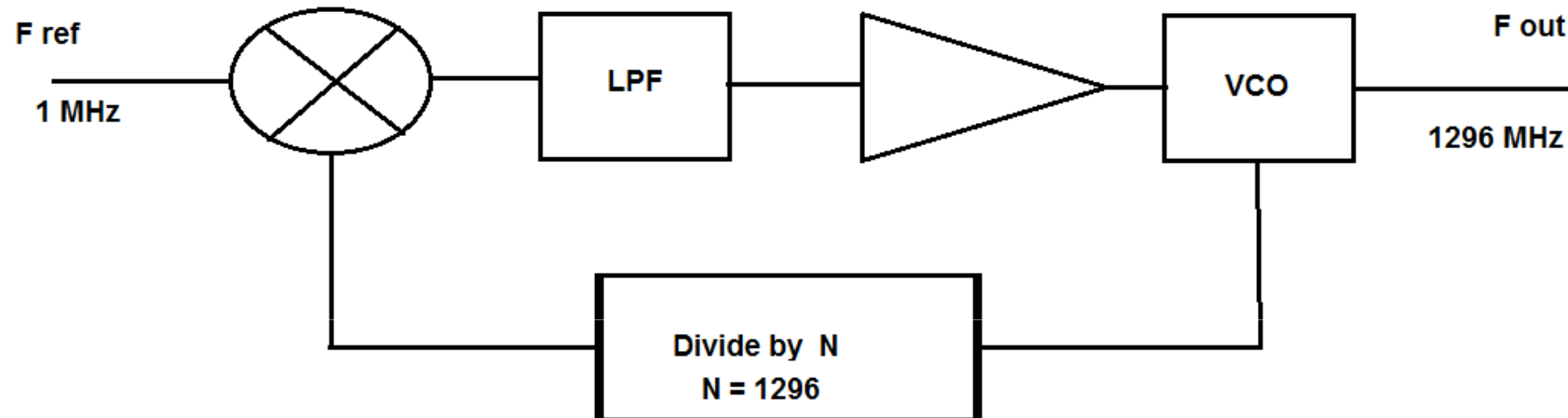
# Integers and Fractional Numbers

- Integers are “whole” numbers, 1, 2, 3, 4... etc
- Fractional numbers are whole numbers with a fractional part, like  $2\frac{1}{3}$  or more generally
- $N = INT + \frac{FRAC}{MOD}$

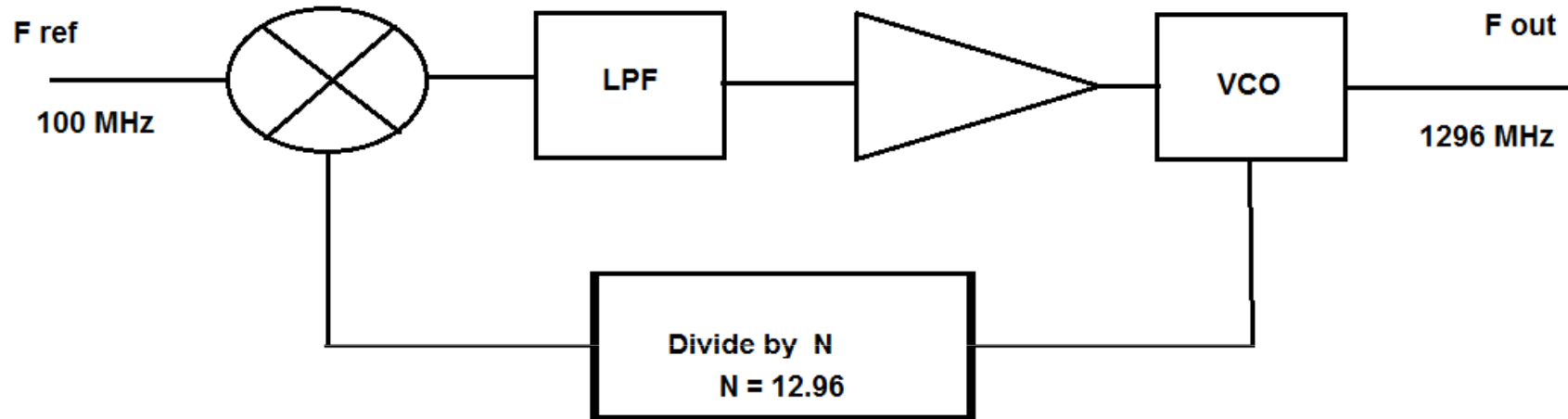
# Fractional-N possibilities

- Can use a higher PFD frequency.
- N can be made a much smaller number.
- Less multiplication of phase noise on reference frequency.
- Useful for PLLs at microwave frequencies.
- Potential for better phase noise performance.
- Allows smaller tuning steps than Int-N.

# Int-N PLL Numerical example



# Frac-N PLL Numerical Example

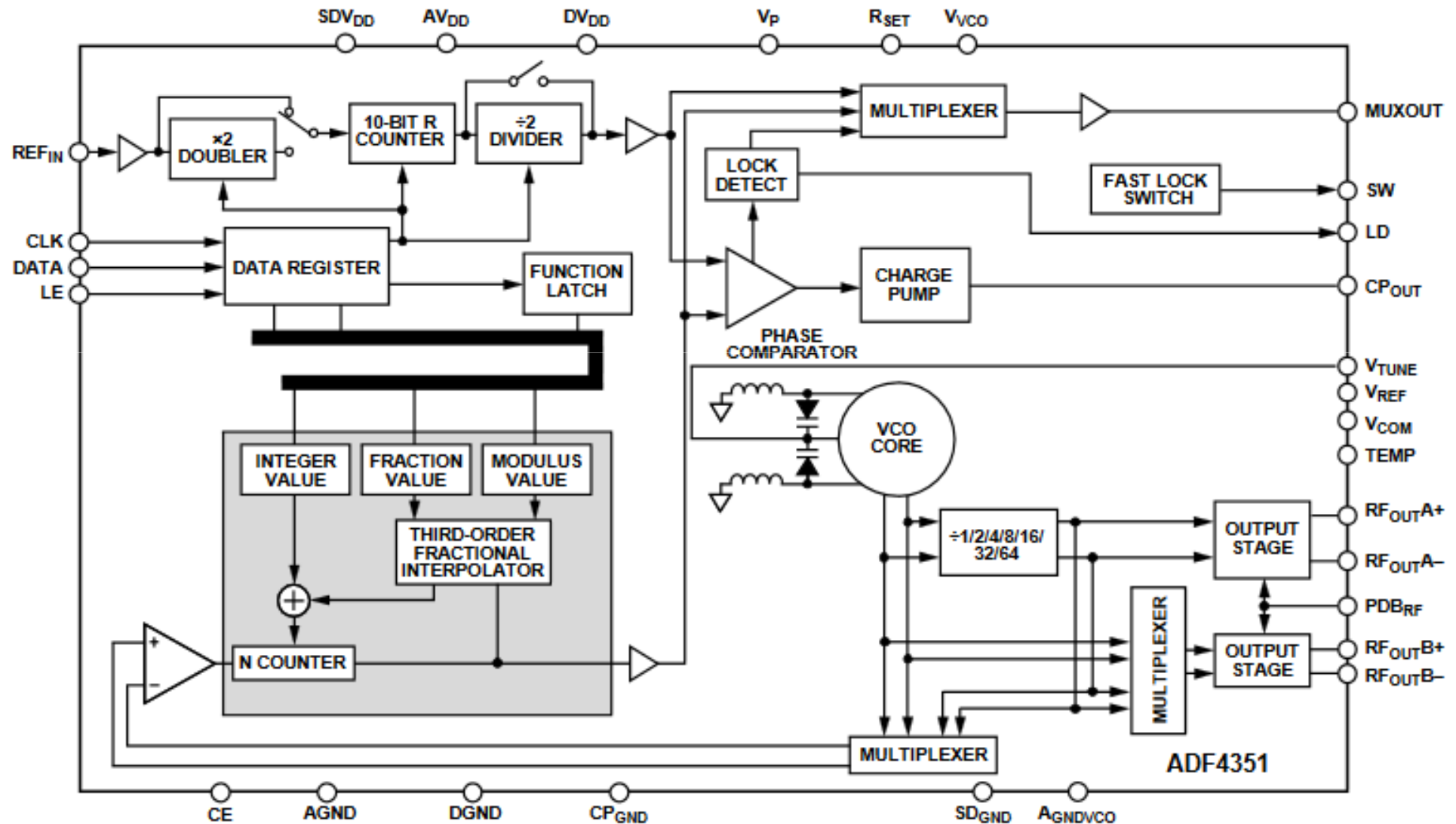


# Implementation of Fractional Divider

- Digital dividers are inherently work with “whole” numbers
- To implement fractional division the divider chain is hopped between two adjacent integer division ratios
- In the foregoing example of  $N = 12.96$  it would divide by 12 and 13, spending 4% of the time dividing by 12 and 96% of the time dividing by 13.



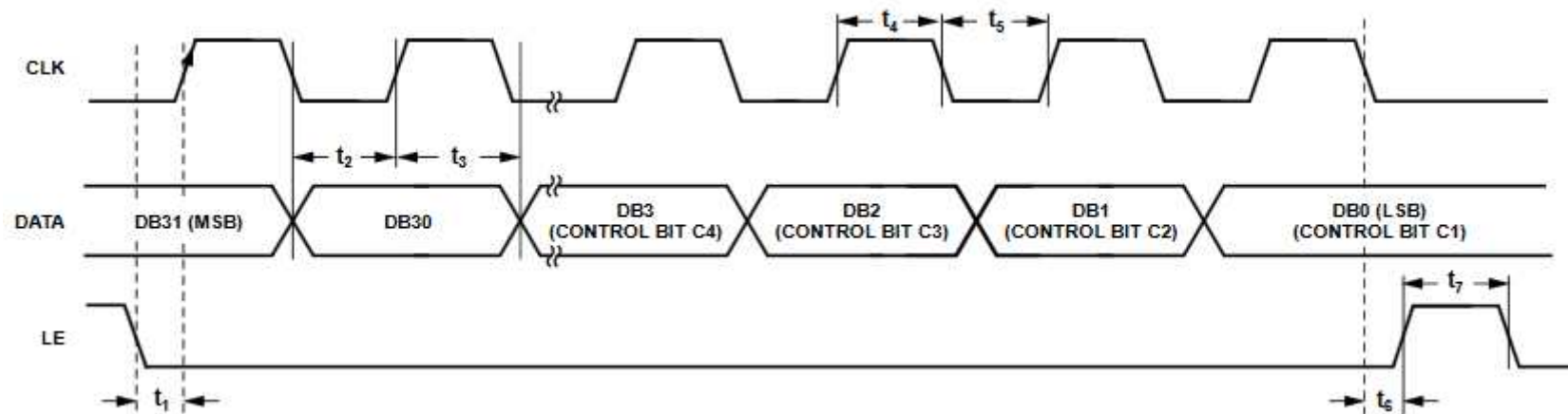
# ADF4351 Block Diagram





# SPI Control Bus

- SPI bus is very standard for the control of ICs.
- A three wire system.
- Clock, Data and LE



# PLL Programming

- ADF4351 has 6 x 32 bit registers to program
- ADF5355 has 13 x 32bit registers to program
- These registers set the frequency, power output, charge pump current etc
- Different approaches are to use Arduinos, PICs or the manufacturers free demo software running on a PC.

# Demo software

**Analog Devices ADF435x Software**

File Tools Help

Select Device and Connection Main Controls Registers Sweep and Hop Other Functions Features

**RF Settings**

**Output**      **VCO**

RF Frequency: 2500    2500 MHz

Channel spacing: 100    100 kHz

Output divider: 1

Reference Frequency: 25 MHz

R counter: 1    Ref Doubler:     Ref /2:

PFD Frequency: 25 MHz

Prescaler: 8/9

Feedback signal: Fundamental    2500 MHz

$$\left( \frac{INT}{100} + \frac{FRAC}{2} \right) \times \frac{PFD \text{ (MHz)}}{N} \div Div = RFout \text{ (MHz)}$$
 INT: 0    PFD (MHz): 25    Div: 1    RFout (MHz): 2500  
 MOD: 2    N = 100

Phase adjust: 0. Off    Phase Value: 1

**Register 2**

Low Noise/Spur Mode: Low noise mode    LDP: 10 ns

Muxout: 3-state output    PD Polarity: Positive

Double buff: Disabled    Powerdown: Disabled

Charge pump current: 2.50    CP 3-state: Disabled

LDF: FRAC-N    Counter reset: Disabled

**Register 3**

Band Select Clock Mode: Low    ABP: 6 ns (FRAC-N)

Charge Cancellation: Disabled    CSR: Disabled

Clock Divider Value: 150

CLK Div Mode: Clock Divider Off

**Register 5**

LD Pin Mode: Digital Lock Detect

**Register 4**

VCO Powerdown: Disabled

MTLD: Disabled

Aux Output Select: Divided

Aux Output Enable: 0. Disabled

Aux Output Power: -4 dBm

RF Output Enable: 1. Enabled

RF Output Power: +5 dBm

**Band Select Clock**

Auto set    Divider: 200

Freq (kHz): 125.000

**Registers**

0x 320000	0x 8008011	0x 4E42	0x 4B3	0x 8C803C	0x 580005	Write All Registers
Write R0	Write R1	Write R2	Write R3	Write R4	Write R5	

Application started.

Device in use: ADF4351  
Software version: 4.5.0

**ANALOG DEVICES**

No device connected

# Demo Software

- Strongly recommend this for getting to know these devices.
- Allows “tweaking” the settings for best performance.
- Designed to go with the demo boards which have a USB interface.
- Need a Cypress CY7C68013A board to do this.
- Fortunately these are only about £5!!

# Cypress CY7C68013A USB2.0 Board

<https://www.ebay.co.uk/itm/EZ-USB-FX2LP-Cypress-CY7C68013A-USB2-0-Development-Board/232072867953?epid=1391320733&hasht>

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# Cypress CY7C68013A USB2.0 Board

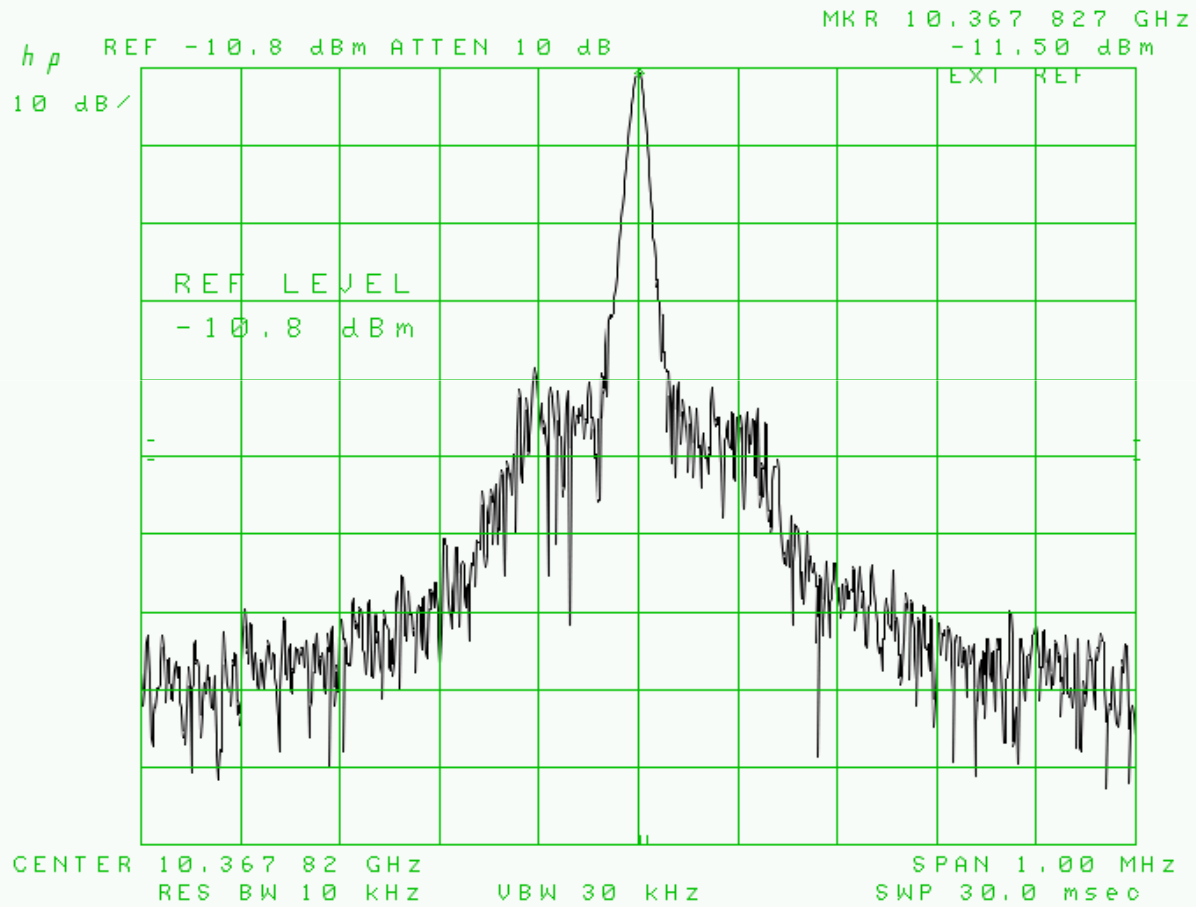
- Need to programme the board with the VID/PID for the AD demo board to fool the PC into thinking it has a real demo board connected so software can run.
- Details at <https://gm8bjf.joomla.com/articles/9-pc-control-of-analog-devices-adf4xxx-synthesiser-chips>



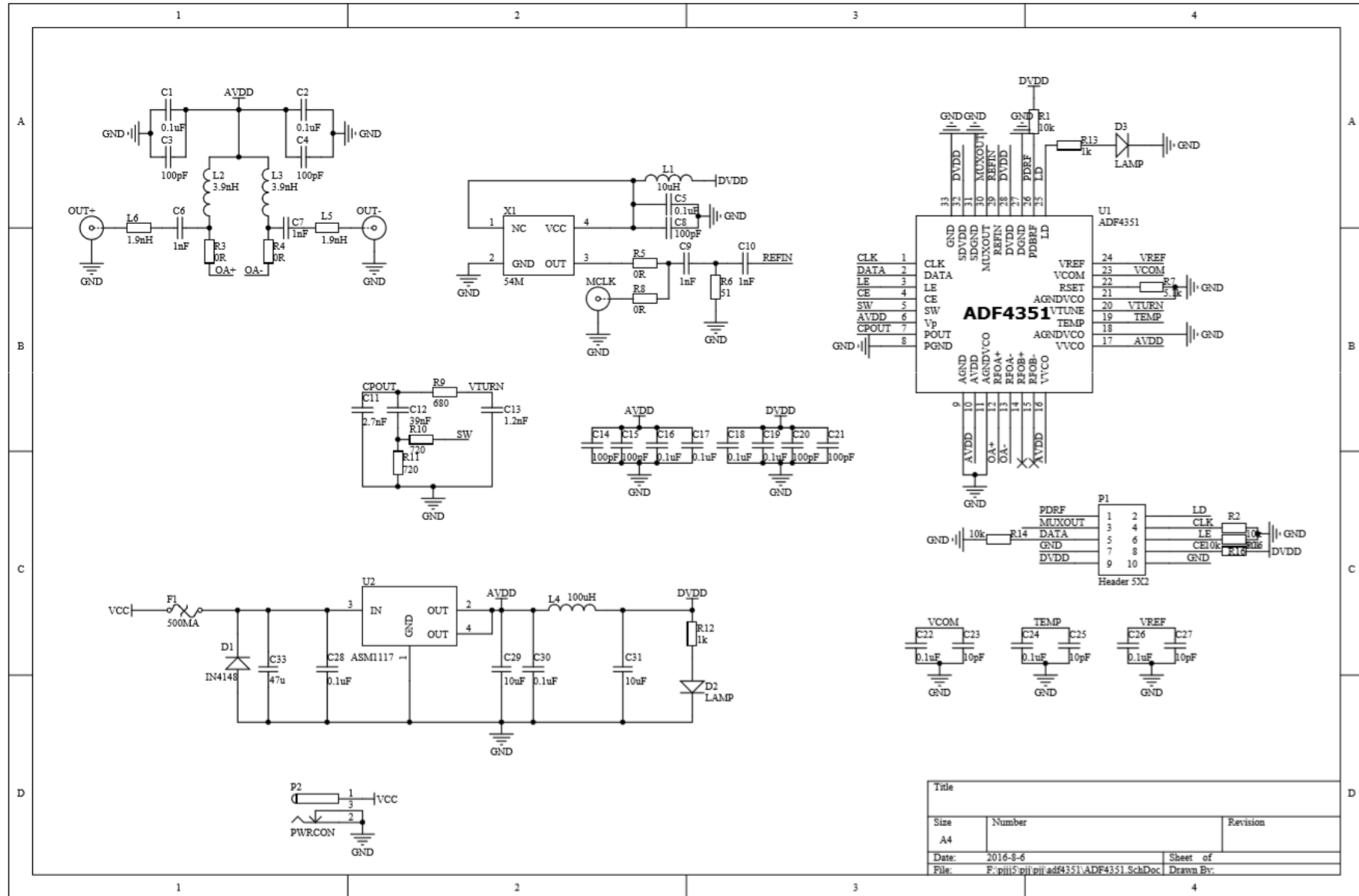
# Phase Noise

- One problem with the low cost Chinese boards is phase noise.
- The RF output is contaminated by noise.
- Comes from poor quality power supply regulators on the boards.
- AD recommends the use of their ultra low noise regulators to power the ADF synthesiser chips.

# Phase Noise



# Schematic for ADF4351 PCB



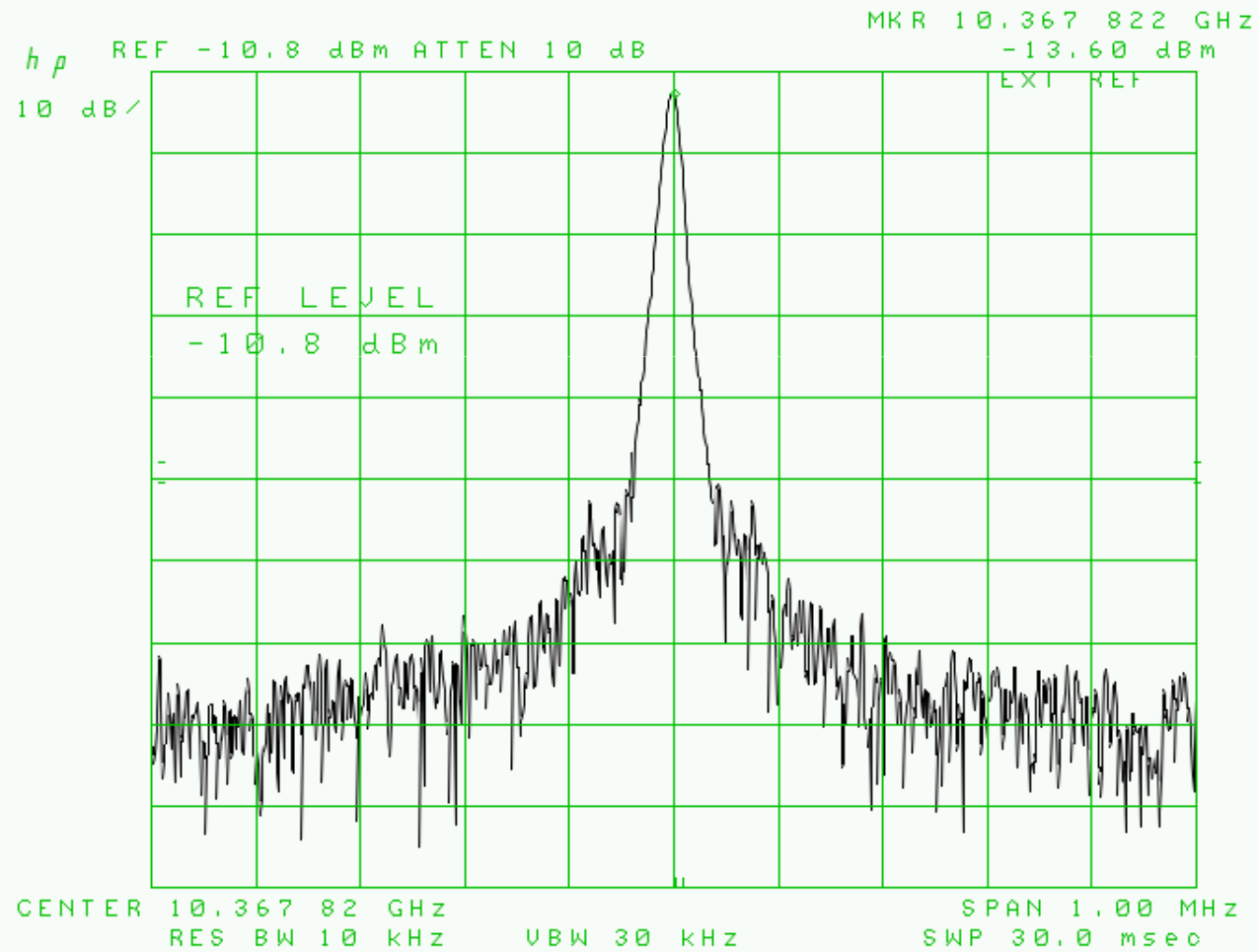
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# Phase Noise

- Two possible solutions
- Use additional decoupling
- Use the AD ultra low noise regulators.
- ADM7150 – Noise performance is 10 dB better than the LT parts used on the Chinese PCBs.
- Package uses the dreaded “Pin 0” so need a custom PCB to make good use of them.

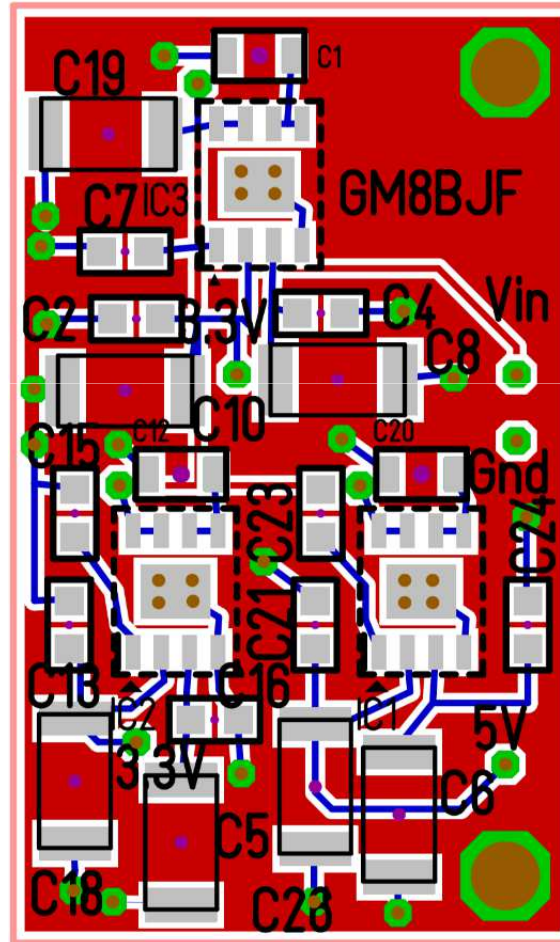
# That's better!





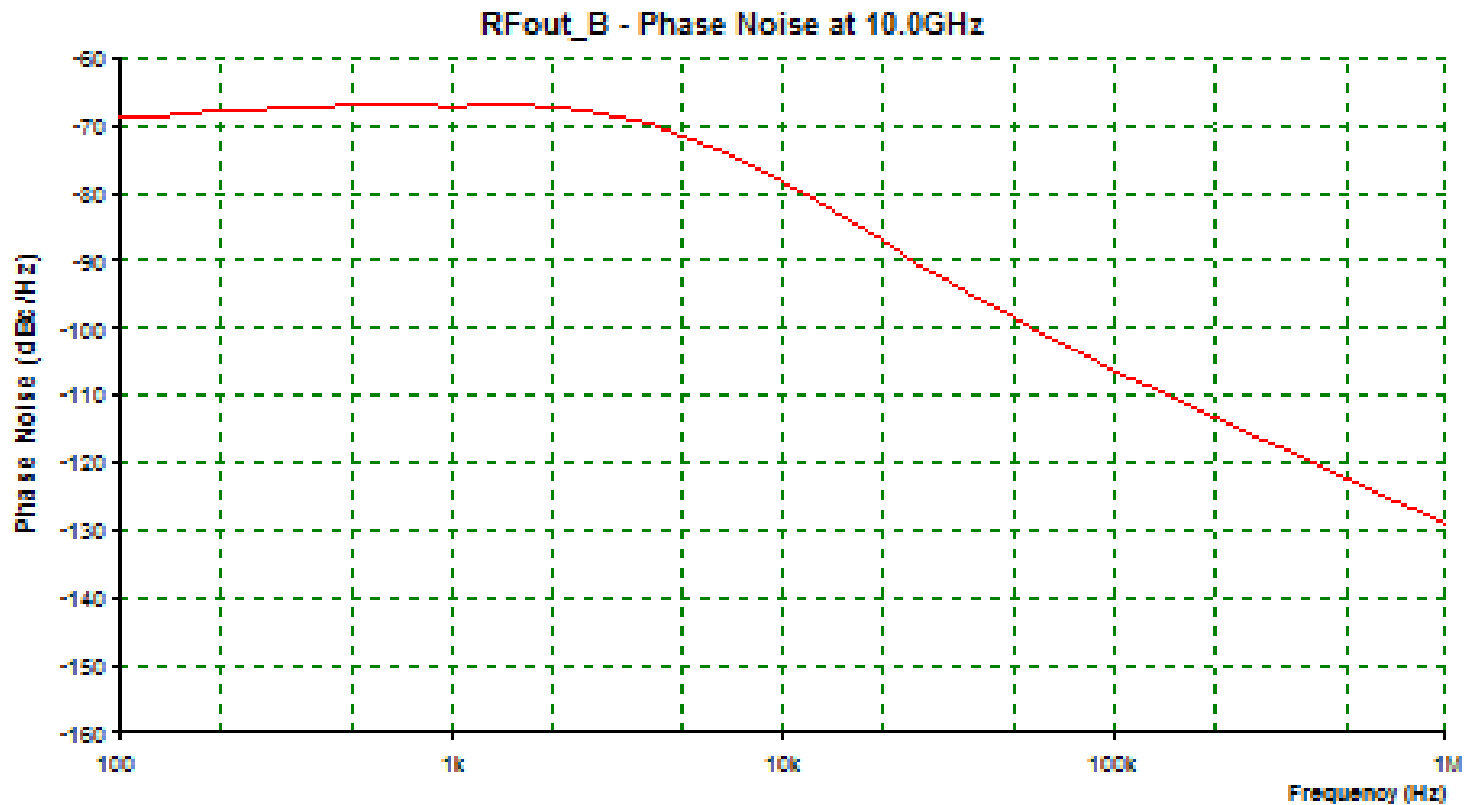


# Regulator PCB

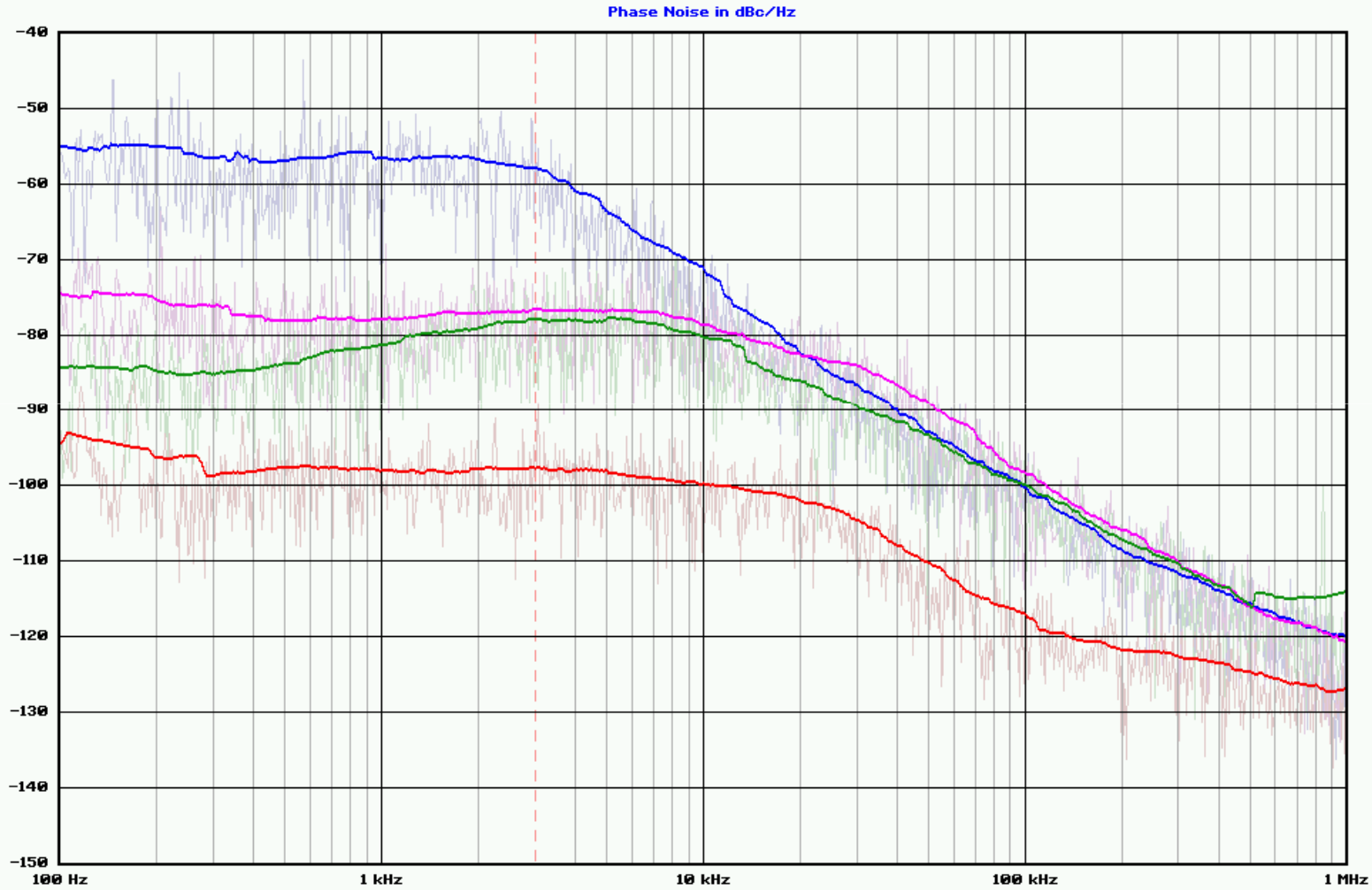




# Simulated Phase noise at 10 GHz



# Phase Noise Plots



Trace	Carrier Hz	Carrier dBm	dBc/Hz at 3000 Hz	Time/Date	Instrument	Rev
adf5355 (Icp=0.3mA) vs CTI-Herley 12.575GHz	575 700 150	-11.20	-57.9	21/12/2017 17:38:14	HP8566B	2639
adf5355 (Icp=4.8mA) vs CTI-Herley 12.575GHz	575 701 250	-11.20	-76.5	21/12/2017 17:42:43	HP8566B	2639
11.6GHz DFS120 vs CTI-Herley 12.575GHz	975 499 000	-14.20	-77.7	21/12/2017 18:12:30	HP8566B	2639
Phase noise floor (100MHz Cal)	100 000 000	-11.20	-97.6	21/12/2017 17:50:26	HP8566B	2639

# Applications

- Local oscillators
- Beacons
- Signal generators
- Test signals
- Weak signal sources
- Etc ...

# Conclusions

- The Chinese PCBs offer a low cost RF source for microwaves.
- They need to be altered to get the best phase noise performance.
- The phase noise performance after modification is as good as the chips are capable of.